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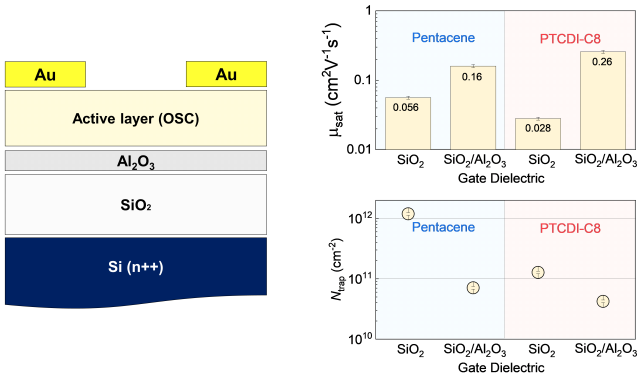
RESEARCH

Low-Voltage n- and p-Channel Organic Transistors using Al_2O_3 Dielectric

Walid Boukhili[1], Swelm Wageh[2], Chee Leong Tan[1], Huabin Sun[1], Dongyoon Khim[1*]

[1]College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210023, China

[2]Department of Physics, Faculty of Science, King Abdulaziz University, Jeddah 21589, Saudi Arabia



ABSTRACT

The integration of high-k dielectric materials presents a promising strategy to reduce the operating voltage of organic thin-film transistors (OTFTs) while enhancing their overall performance. In this study, we explore the impact of a 20 nm Al_2O_3 interlayer deposited atop conventional SiO_2 dielectrics on the electrical characteristics of both p-channel pentacene and n-channel N,N′-dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C8) OTFTs. Devices incorporating the Al_2O_3/SiO_2 bilayer dielectric demonstrate marked improvements in electrical properties for both n-type and p-type devices, including increased drain current, transconductance, and carrier mobility, along with higher on/off current ratios at reduced operating voltages compared to those using SiO_2 alone. Furthermore, this bilayer architecture lowers threshold and turn-on voltages, decreases subthreshold swing, and mitigates interfacial trap states and contact resistance, thereby promoting more efficient charge injection and enhanced device operation across both charge carrier types. These findings highlight the effectiveness of Al_2O_3/SiO_2 dielectric engineering as a viable approach for advancing low-power, high-performance organic electronics.

Key Words: OTFTs, High-k dielectric, Low voltage, Interface trap state, Contact resistance

*Correspondence: dongyoonkhim@njupt.edu.cn

1. INTRODUCTION

Organic thin-film transistors (OTFTs) have attracted significant attention as promising candidates for next-generation flexible, low-cost, and large-area electronic applications [1-8]. However, achieving low operating voltages and high performance simultaneously remains a critical challenge, largely limited by the dielectric layer's properties and the organic semiconductor/dielectric interface [9-12]. Furthermore, the interfacial properties between the organic semiconductor and dielectric critically influence charge transport and overall device performance. Engineering and optimizing these interfaces are essential to realize high-performance OTFTs with stable and efficient operation [9-12]. Extensive efforts have been devoted to enhancing OTFT performance, particularly by achieving low-voltage operation through diverse processing strategies [13-24]. Conventional low-k dielectric materials such as silicon dioxide (SiO_2), with a dielectric constant of ~3.9 [18,24], inherently limit gate capacitance at a given thickness, thereby requiring high operating voltages that are unsuitable for low-power applications. On the other hand, integrating high-k dielectrics such as aluminum oxide (Al_2O_3), with a dielectric constant between 6 and 9 [18, 24], provides a promising approach to overcome these limitations by increasing gate capacitance, thereby reducing operating voltages and improving charge modulation [18,24]. While high-k Al_2O_3 is widely used in inorganic electronics [21,22], its application in OTFTs remains limited, particularly in configurations that avoid complex surface treatments. This is largely due to the sensitivity of organic semiconductors to interfacial disorder, which can introduce trap states and degrade device performance. This gap highlights the need to investigate simplified high-k dielectric strategies that ensure favorable interface characteristics while enhancing OTFT performance. In this regard, engineering bilayer dielectric stacks by integrating high-k Al_2O_3 atop SiO_2 offers a promising route to improve dielectric function and interfacial compatibility without relying on surface modifications or self-assembled monolayers (SAM). This approach may enable high-performance, low-power p- and n-type OTFTs for future flexible and wearable electronics.

Herein, we systematically investigate the effect of integrating a high-k Al_2O_3 layer into the gate dielectric stack on hole and electron transport in OTFTs. We directly compare devices using conventional low-k SiO_2 and high-k Al_2O_3/SiO_2 bilayers, with p-channel pentacene and n-channel N, N′-dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C8) as the active layers. ll transistors were fabricated and characterized without any surface treatments or self-assembled monolayers (SAM) on the dielectric surface to investigate the intrinsic nature of Al_2O_3. Our detailed evaluation of a 20-nm Al_2O_3 layer shows significant improvement in electrical performance for both charge carrier types. In particular, devices with the Al_2O_3/SiO_2 bilayer operate within ±10 V and exhibit markedly enhanced key device parameters compared to those with SiO_2. This dielectric engineering approach offers a clear pathway to low-power, high-performance OTFTs by increasing the dielectric constant and improving the semiconductor/dielectric interface.

2. MATERIALS AND METHODS

All chemicals used in this study were purchased from

Sigma-Aldrich and used without further purification. The schematic cross-section of the bottom-gate, top-contact OTFT structure fabricated in this work is shown in Fig. 1(a). The energy levels, including the Fermi level of Au, and the HOMO and LUMO levels of pentacene and PTCDI-C8, along with the molecular structures of pentacene and PTCDI-C8, are shown Fig. 1(b). OTFTs were fabricated on heavily n-doped Si wafers serving as both the substrate and gate electrode, coated with a 200 nm thermally grown SiO_2 gate dielectric. Prior to organic layer deposition, substrates were ultrasonically cleaned in acetone, isopropanol, and deionized water, followed by UV/ozone treatment (20 min) and nitrogen drying (5 min). Two gate dielectric configurations were employed: a single-layer low-k SiO_2 (200 nm) and a bilayer high-k Al_2O_3 (20 nm)/low-k SiO_2 (200 nm). For the bilayer structure, a 20 nm Al_2O_3 layer was deposited by atomic layer deposition (ALD) atop the SiO_2 dielectric, which served as the initial dielectric layer. The ALD process was conducted at 150℃ using trimethylaluminum (TMA) as the metal precursor and water vapor as the oxidant. Depositions proceeded through alternating, self-limiting exposures to TMA and H_2O, resulting in a growth rate of approximately 1.1 Å per cycle. Pentacene and PTCDI-C8 were thermally evaporated as p- and n-type organic semiconductors, respectively, at 0.05 nm/s under 5×10^{-6} mbar vacuum, to a thickness of 50 nm. Gold (Au) source and drain (S–D) electrodes (80 nm) were then deposited through a shadow mask, defining a channel length (L) of 50 μm and width (W) of 2,000 μm. All electrical characterizations of the OTFTs were conducted in the dark under vacuum (~10^{-1} mbar) using a Keithley HP 5156 semiconductor characterization system.

3. RESULTS AND DISCUSSION

Table 1 summarizes the dielectric type, dielectric constant, capacitance per unit area, bandgap energy, and thickness of each gate dielectric [18,24]. The equivalent total capacitance of the Al_2O_3/SiO_2 bilayer dielectric was calculated using the series capacitance

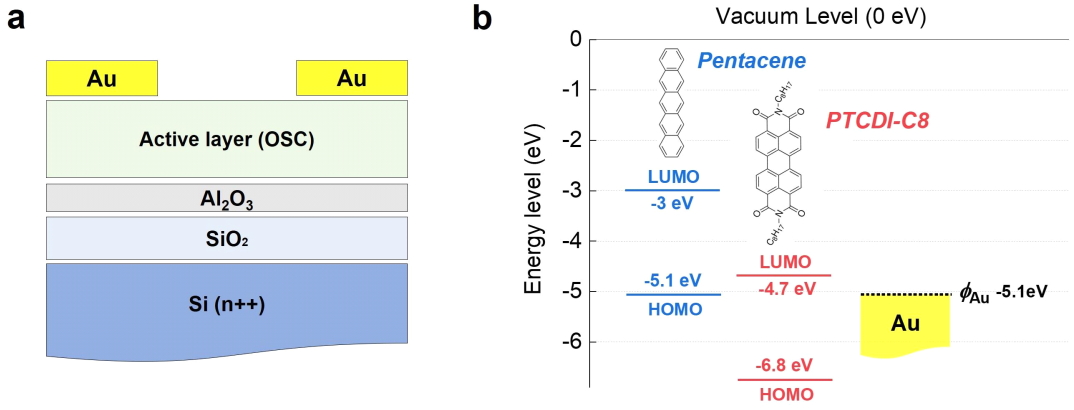


Fig. 1. (a) A schematic cross-section of the bottom-gate, top-contact OTFT structure. (b) Energy level diagram showing the Fermi level of Au and the HOMO/LUMO levels of pentacene and PTCDI-C8, along with the molecular structures of both materials.

Table 1. Type, dielectric constant, capacitance per unit area, band gap energy, and thickness of the gate dielectrics used, adapted from Refs. [18,24]

Dielectric materials	k-type	Dielectric constant	Capacitance ($nFcm^{-2}$)	Band gap (eV)	Thickness (nm)
Silicon oxide (SiO_2)	low-k	3.9	8.3	9	200
Aluminum oxide (Al_2O_3)	high-k	9	165	8.8	20
Al_2O_3/SiO_2	high-k /low-k	–	7.9	–	220

model according to:

$$C_{eq} = \frac{1}{C_{Al_2O_3}} + \frac{1}{C_{SiO_2}} \quad (1)$$

where the individual areal capacitances of Al_2O_3 and SiO_2 are given in Table 1. Based on this relation, the equivalent capacitance C_{eq} of the bilayer dielectric was calculated to be approximately 7.9 $nFcm^{-2}$.

Fig. 2(a)–(b) shows the transfer characteristics (I_d–V_g) and transconductance (g_m) as a function of V_g in the linear regime for p-channel (V_d=−10 V) and n-channel (V_d=+10V) OTFTs with SiO_2 gate dielectric, respectively. Meanwhile, Fig. 2(c)–(d) displays the corresponding characteristics for p-channel (V_d=−1 V) and n-channel (V_d=+1 V) OTFTs with Al_2O_3 (20 nm)/SiO_2 (200 nm) bilayer gate dielectric, respectively. As shown in Fig. 2(a)–(d), a clear difference in device performance is observed between p- and n-channel OTFTs with SiO_2 (200 nm) and those with Al_2O_3 (20 nm)/SiO_2 (200 nm) bilayer dielectric.

Devices with SiO_2 required higher operating voltages and exhibited lower drain currents. In contrast, incorporating a 20 nm Al_2O_3 interlayer significantly enhanced the drain current, reaching −1.55×10^{-5} A for p-channel and 2.37×10^{-5} A for n-channel devices at relatively low voltages.

Transconductance (g_m), which quantifies the modulation of I_d as a function of V_g at a constant V_d, is calculated using [25,26]:

$$g_m = \left[\frac{\delta I_D}{\delta V_G}\right]_{V_{D=cte}} = \frac{W}{L}\mu lin C_i V_d \quad (2)$$

where μ_{lin} is the linear mobility, C_i is the capacitance of the insulator per unit area, and W and L represent the channel width and length, respectively.

To ensure a fair device performance comparison, the extrapolation in the linear region (ELR) method [27,28] was employed to extract the maximum drain current ($I_{d,max}$), the gate voltage at peak transconductance ($V_{g,max}$), and the maximum transconductance ($g_{m,max}$) from the transfer and transconductance characteristics in the linear regime of each device, as illustrated in Fig. 2(c). The extracted values of $V_{g,max}$ and $g_{m,max}$ are plotted as a function of $I_{d,max}$ in Fig. 2(e)–(f). Interestingly, both p- and n-channel OTFTs with a Al_2O_3/SiO_2 dielectric exhibited significantly higher $g_{m,max}$ values, 1.2×10^{-6} S (p-channel) and 8.6×10^{-7} S (n-channel), under low $V_{g,max}$, compared to 5.2×10^{-8} S and 5.4×10^{-7} S, respectively, for devices with SiO_2, confirming the enhanced performance.

These behaviors are mainly attributed to the enhanced charge storage capability at the conductive channel/dielectric interface, where the Al_2O_3/SiO_2 bilayer enables efficient charge carrier accumulation at low operating voltages, leading to increased I_d and g_m.

Furthermore, the measured g_m increases quasi-linearly

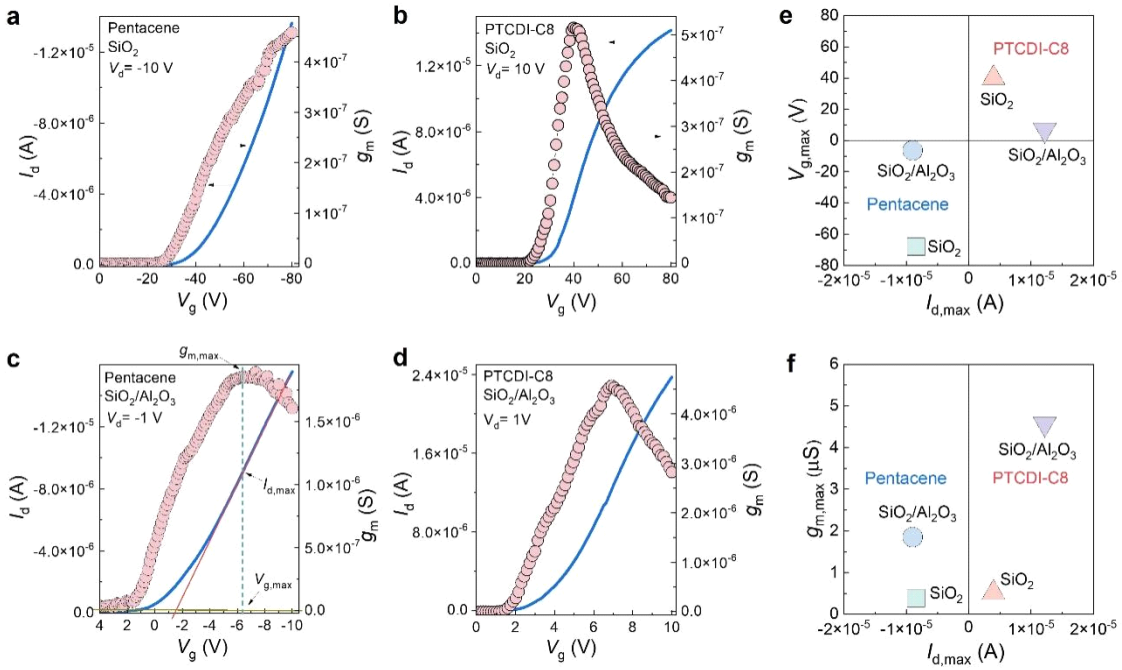


Fig. 2. (a,b) Transfer characteristics (I_d–V_g) and transconductance (g_m) as a function of gate voltage (V_g) in the linear regime for p-channel (V_d=–10 V) and n-channel (V_d=+10 V) OTFTs with a SiO_2 gate dielectric. (c,d) Corresponding characteristics for p-channel (V_d=–1 V) and n-channel (V_d=+1 V) OTFTs with an Al_2O_3 (20 nm)/SiO_2 (200 nm) bilayer gate dielectric. (e,f) extracted $V_{g,max}$ and $g_{m,max}$ values plotted as a function of $I_{d,max}$.

with V_g and decreases at high V_g, as can be seen in Fig. 2(b)–(d). Presumably, the decrease in g_m at high V_g results from the presence of contact resistance (R_c) at the S–D electrodes/organic semiconductor interface [25, 29].

Fig. 3(a)–(d) presents the transfer characteristics (I_d–V_g, left axis) and the square root of the drain current versus gate voltage (–V_g, right axis) in the saturation regime for both p-channel and n-channel OTFTs. The comparison includes devices with a SiO_2 dielectric operated at ±80 V and those with an Al_2O_3/SiO_2 bilayer dielectric operated at ±10 V. As shown in Fig. 3(c)–(d), both p-channel and n-channel OTFTs incorporating the Al_2O_3/SiO_2 bilayer operate reliably at a low voltage of ±10 V, attributed to the high dielectric constant of the inserted Al_2O_3 layer. In contrast, devices with SiO_2 alone require a higher operating voltage (±80 V) to achieve similar electrical performance. A maximum I_d level of -3×10^{-5} A at −10 V was achieved for the p-channel OTFT, while the n-channel device exhibited 3.75×10^{-5} A at +10 V, both employing the Al_2O_3/SiO_2 bilayer dielectric. In contrast, at the same operating gate voltages (−10 V for p-channel and +10 V for n-channel), devices with SiO_2 exhibited significantly lower drain currents of -2.6×10^{-5} A and 1.84×10^{-5} A, respectively.

It can be concluded that the use of an Al_2O_3 interlayer on SiO_2 effectively enables high saturation current operation at low voltage for both p-channel and n-channel OTFTs, outperforming devices with SiO_2.

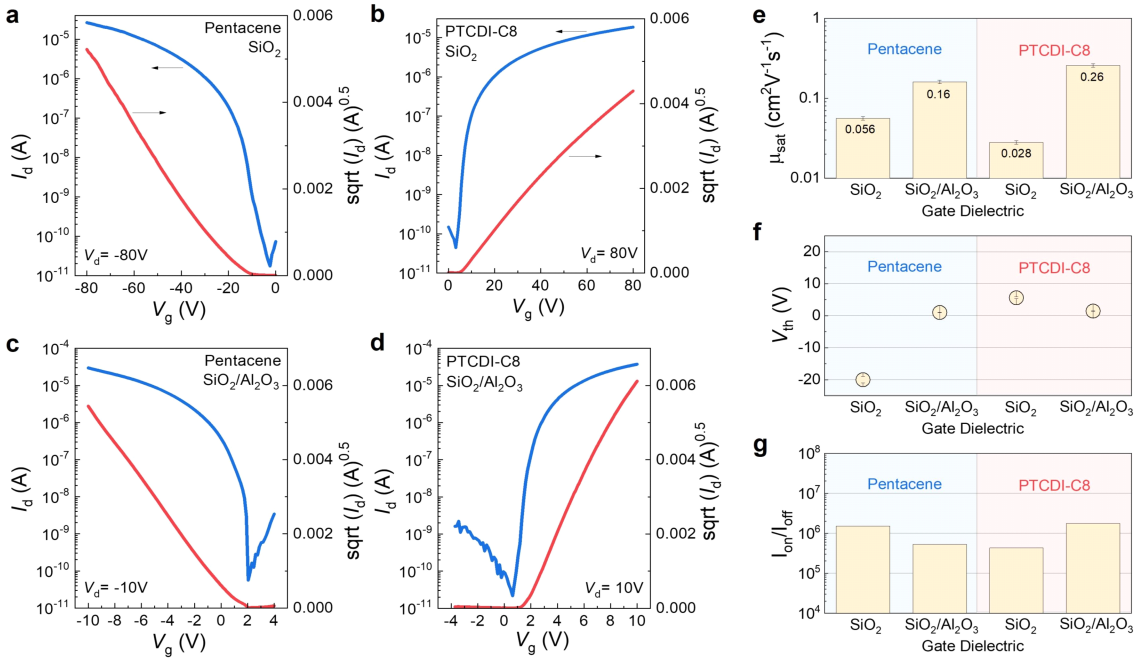


Fig. 3. (a–d) Transfer characteristics (I_d–V_g, left axis) and $\sqrt{I_d}-V_g$ plots (right axis) in the saturation regime for p-channel and n-channel OTFTs. Corresponding extracted values of: (e) Maximum saturation mobility ($\mu_{sat,max}$). (f) Threshold voltage (V_{th}). (g) Current on/off ratios (I_{on}/I_{off}).

In the saturation regime, the mobility is extracted using the following equation [25,26]:

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_d}}{\partial V_g}\right)^2 \quad (3)$$

The threshold voltage (V_{th}) for each device was extracted by linearly fitting the square root of the transfer characteristics ($\sqrt{I_d}$–V_g) in the saturation regime and extrapolating to zero drain current.

The maximum saturation mobility values ($\mu_{sat,\ max}$) for all devices are shown in Fig. 3(e), while the obtained V_{th} values are presented in Fig. 3(f). As shown in Fig. 3(e), the highest mobility values were obtained from devices with the Al_2O_3/SiO_2 bilayer dielectric, reaching 0.26 $cm^2\ V^{-1}\ s^{-1}$ for n-channel and 0.16 $cm^2\ V^{-1}\ s^{-1}$ for p-channel OTFTs, compared to 0.028 and 0.056 $cm^2\ V^{-1}\ s^{-1}$, respectively, for devices with SiO_2.

Devices employing a Al_2O_3/SiO_2 bilayer dielectric exhibit near zero V_{th}, measured at approximately 1.0 V for p-channel and 1.46 V for n-channel OTFTs, in contrast to devices with a SiO_2 dielectric, which show significantly higher V_{th} values of −20 V and 5.6 V, respectively. Such low V_{th} is crucial for the integration of OTFTs into low-voltage circuits [30]. The observed difference in V_{th} between SiO_2-based and Al_2O_3/SiO_2-based devices underscores the strong influence of dielectric composition on device behavior.

The current on/off ratios (I_{on}/I_{off}) for all devices are also extracted from the I_d–V_g characteristics in the saturation regime and are presented in Fig. 3(g). Among all devices studied, the n-channel transistor

with a 20-nm Al_2O_3 insertion layer exhibits the highest I_{on}/I_{off} ratio of 1.736×10^6, significantly improved compared to the device with SiO_2, which shows a ratio of 4.263×10^5.

In contrast, the p-channel device shows a decrease in I_{on}/I_{off} when Al_2O_3 is incorporated atop SiO_2.

Next, the turn-on voltage (V_{on}) refers to the gate voltage at which a conductive channel begins to form between the S–D electrodes [31]. Fig. 4(a) shows the measured values of V_{on} for all devices. Remarkably, all the V_{on} values were notably low, suggesting a better gate voltage modulation. Therefore, the low V_{on} values observed in our p- and n-channel OTFTs are advantageous and comparatively lower than those previously reported in other OTFTs [28,32].

The enhanced performance of both p- and n-channel OTFTs is attributed to the improved interfacial properties introduced by the high-k Al_2O_3 layer, along with the advantage of its high dielectric constant, which enhances electrostatic control and enables lower operating voltages. This high-k layer likely reduces the interfacial trap density, resulting in higher drain current, enhanced saturation mobility, and reduced V_{th}, and V_{on}. To further investigate this effect, interface trap densities were systematically extracted for all devices across both lower and higher energy regions.

In OTFT devices, the trap density at the dielectric/OSC interface, along with structural disorder in the semiconductor, is often suggested to influence the V_{th}, V_{on}, and SS [33,34]. Here, two independent approaches were employed to estimate the trap densities associated with each dielectric layer.

The first approach estimates the interfacial trap density (N_{tr}) based on the measured V_{th} and V_{on}, providing insight into trap-related interfacial characteristics, as given by the following equation [35]:

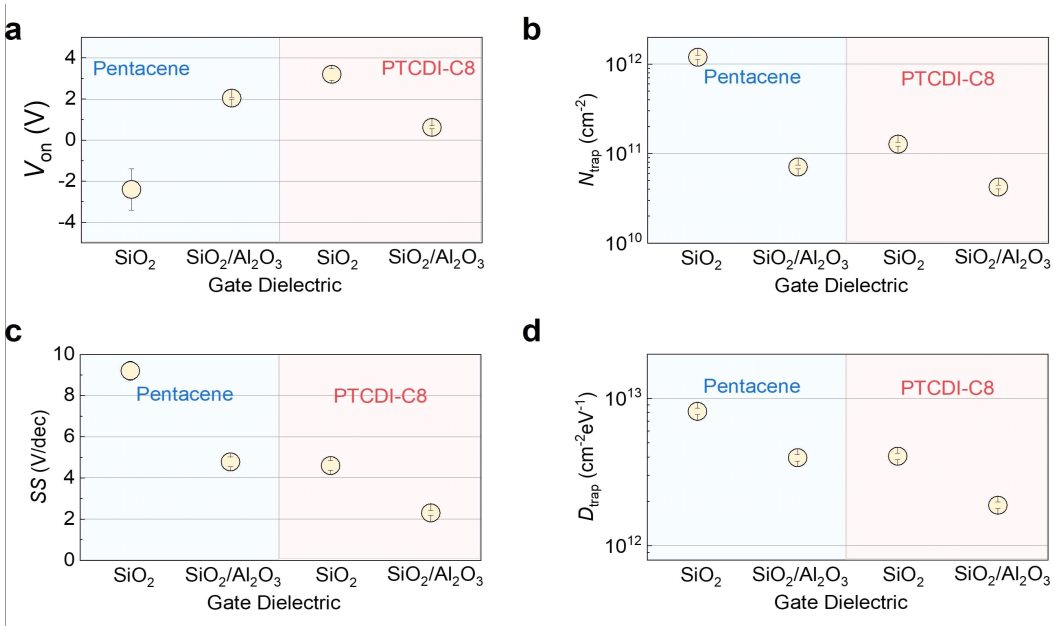


Fig. 4. Extracted values of: (a) Turn-on voltage (V_{on}). (b) Trap density (N_{tr}). (c) Subthreshold swing (SS). (d) Interface trap density (D_{it}) of p-channel and n-channel OTFTs.

$$N_{tr} = \frac{C_i \left| V_{th} - V_{on} \right|}{q} \quad (4)$$

The calculated N_{tr} values are presented in Fig. 4(b). Notably, the highest extracted trap state densities (N_{tr}) were 1.2×10^{12} cm^{-2} for p-channel and 1.275×10^{11} cm^{-2} for n-channel OTFTs employing SiO_2 as the gate dielectric. In contrast, the lowest N_{tr} values were 7×10^{10} cm^{-2} for p-channel and 4.23×10^{10} cm^{-2} for n-channel devices with the Al_2O_3/SiO_2 bilayer. These results indicate that both p- and n-channel OTFTs with Al_2O_3/SiO_2 dielectrics exhibit low trap state densities near to the Fermi level [36], corresponding to the low-energy region.

In this second approach, the interface trap density (D_{it}) is extracted from the *SS* values using the following expression [29, 35]:

$$D_{it} = \left[\frac{SSlog(e)}{k\,T/q} - 1 \right] \frac{C_i}{q} \quad (5)$$

where T is the temperature, k is Boltzmann's constant, q is the elementary charge, and SS is the subthreshold swing. *SS* serves as a key indicator of device performance and is directly influenced by the trap density at the organic semiconductor (OSC)/gate dielectric interface. It can be extracted from the transfer characteristics using [29]:

$$SS = \frac{d\,V_g}{dlog(I_d)} \quad (6)$$

The calculated *SS* and D_{it} values are presented in Fig. 4(c), Fig. 4(d), respectively. Although the second method also examines trap states near the Fermi level, it is mainly used to extract the trap state density per unit energy at higher energy levels beyond the range covered by the first method. Fig. 4(d) shows relatively high interface trap densities at higher energy levels, with values of 8.15×10^{12} cm^{-2} eV^{-1} (p-channel) and 4.05×10^{12} cm^{-2} eV^{-1} (n-channel) for SiO_2 devices, which are reduced to 3.95×10^{12} cm^{-2} eV^{-1} and 1.88×10^{12} cm^{-2} eV^{-1}, respectively, in devices using the Al_2O_3/SiO_2 bilayer. These findings indicate that the differences in electrical performance are primarily influenced by deep trap states located closer to the highest occupied molecular orbital (HOMO) in p-channel devices and the lowest unoccupied molecular orbital (LUMO) in n-channel devices, suggesting that trap states in the high-energy region have a greater impact than those in the low-energy region.

Fig. 5(a), Fig. 5(b) shows the output characteristics (I_d–V_d) of p-channel and n-channel OTFTs with a SiO_2 gate dielectric, while Fig. 5(c), Fig. 5(d) displays the corresponding characteristics of devices employing an Al_2O_3/SiO_2 bilayer dielectric. As shown in Fig. 5(c), Fig. 5(d), the incorporation of a 20 nm high-k Al_2O_3 layer enables both p- and n-channel OTFTs to operate at low voltages (±10 V), compared to the higher voltage requirements of devices using SiO_2. All devices exhibit a clear transition from the linear to the saturation regime, where I_d increases linearly at low V_d and saturates at higher V_d due to channel pinch-off. The introduction of the Al_2O_3 layer enhances the I_d level at low applied drain and gate voltages, as evidenced by the output characteristics. This result further confirms that the Al_2O_3/SiO_2 bilayer dielectric improves the semiconductor/dielectric interface, facilitating more efficient charge transport and leading to higher I_d levels.

R_c can significantly hinder charge injection, thereby limiting the overall performance of OTFTs [28,37,38]. Understanding its impact on carrier injection from the S–D electrodes to the conductive channel is essential

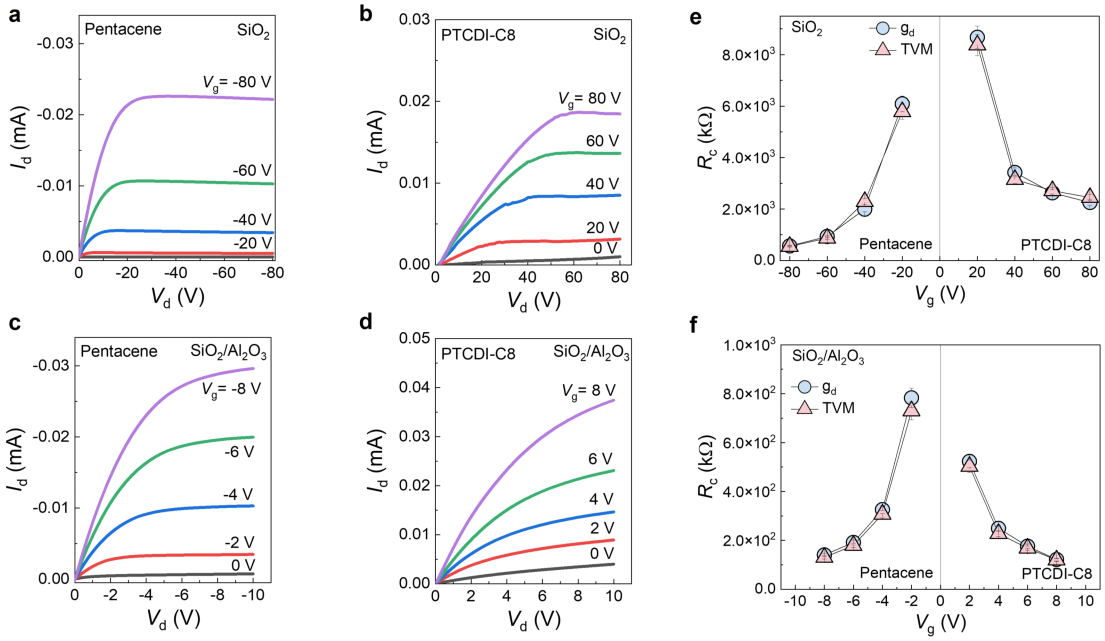


Fig. 5. (a–b) Output characteristics (I_d–V_d) of p-channel and n-channel OTFTs with a SiO_2 gate dielectric. (c–d) Corresponding characteristics of devices with an Al_2O_3/SiO_2 bilayer gate dielectric. (e–f) Contact resistance (R_c) values extracted using both methods as a function of V_g.

for optimizing device efficiency. Several methods have been developed to extract R_c, including the Y-function method, the transfer line method (TLM), the transition voltage method (TVM), and the output conductance method [28,37,38]. Herein, the influence of the dielectric on contact resistance was assessed using two complementary methods: the transition voltage method (TVM) and the conductance method, both of which were employed to accurately extract R_c of the investigated OTFTs.

At low drain voltage, the output conductance of the devices can be expressed as follows [39]:

$$g_d = \frac{1}{R_{tot}} = \left[\frac{\delta I_d}{\delta V_d}\right] V_{g=cte} \tag{7}$$

For each device and at each V_g, the total source-drain resistance (R_{tot}) is extracted from the slope of the linear region of the I_d-V_d output curve, using $R_{tot} = \left[\frac{\delta V_d}{\delta I_d}\right] V_{g-cte}$.

R_c can be extracted as follows:

$$R_C = \frac{1}{g_d} - \frac{L}{WC_i\mu_{FE,lin}(V_g - V_{th})} \tag{8}$$

In addition, an alternative method to extract R_c is the transition voltage method (TVM), where it is expressed as follows [28]:

$$R_C = 2\frac{\sqrt{V_g - V_{th}}\left[\sqrt{2V_{tr}} - \sqrt{V_g - V_{th}}\right]}{I_{sat}} \tag{9}$$

Where, V_{tr} is the transition voltage from linear to saturation regime in the output characteristics, and I_{sat} is the saturation drain current. At a given V_g, V_d=V_{tr} and I_{lin}=I_{sat}. The V_{tr} and I_{sat} values are derived from the

intersection of the two slopes in the linear and saturation regimes of the output characteristics. The extracted R_c values of all p- and n-channel OTFTs with SiO_2 and Al_2O_3/SiO_2 bilayer dielectrics are plotted as a function of V_G in Fig. 5(e)–(f), respectively. Notably, the R_c values obtained from both methods show a good agreement, underscoring the reliability of the analysis, as demonstrated in Fig. 5(e)–(f). The extracted R_c values at high V_G=±80 V for OTFTs employing SiO_2 as the gate dielectric are 5.68×10^2 kΩ for the p-channel pentacene device and 2.25×10^3 kΩ for the n-channel PTCDI-C8 device. Upon introducing a 20 nm high-k Al_2O_3 layer atop the SiO_2 dielectric, R_c values decrease substantially for both device types. For the p-channel device, R_c is reduced to 1.4×10^2 kΩ, while the n-channel device shows a further decrease to 1.2×10^2 kΩ, both measured at V_G=±8 V. Under these conditions, both devices exhibit comparable R_c values. The reduction in R_c observed in devices with Al_2O_3/SiO_2 compared to those with SiO_2 alone is likely attributed to a lower trap density at the semiconductor/dielectric interface, which promotes more efficient charge carrier transport owing to the beneficial influence of the additional high-k Al_2O_3 layer.

The comparative analysis of electrical characteristics of both p-channel and n-channel OTFTs with SiO_2 and Al_2O_3/SiO_2 gate dielectrics reveals a consistent and compelling trend of performance enhancement across all metrics, underscoring the effectiveness of the bilayer dielectric strategy. Devices employing the Al_2O_3/SiO_2 bilayer exhibit superior performance, marked by higher μ_{sat}, steeper SS, lower trap densities, and reduced R_c compared to their SiO_2 counterparts. These improvements are mainly attributed to the dual benefits of the high-k Al_2O_3 layer: (i) enhanced electrostatic control due to the increased dielectric constant, which enables efficient charge carrier accumulation at low operating voltages, and (ii) a reduction in interface trap states at the semiconductor–dielectric interface, facilitating more efficient charge transport. Importantly, these enhancements were achieved without any surface treatments or SAMs, underscoring the intrinsic ability of high-k Al_2O_3 to form a favorable and trap-minimized interface with organic active layers. These results further underscore the effectiveness of this dielectric engineering strategy in advancing low-power, high-performance organic electronics.

4. CONCLUSION

In summary, p-channel pentacene and n-channel PTCDI-C8 OTFTs were fabricated using either a SiO_2 dielectric or Al_2O_3/SiO_2 bilayer. The bilayer dielectric effectively lowers the operating voltage to ±10 V while improving charge transport, thereby significantly enhancing overall device performance. Devices with Al_2O_3/SiO_2 show improved mobility (0.16 $cm^2V^{-1}s^{-1}$ for holes and 0.26 $cm^2V^{-1}s^{-1}$ for electrons), higher transconductance, near-zero V_{th} and V_{on}, and higher on/off current ratios. The Al_2O_3 layer also significantly lowers R_c (1.4×10^2 kΩ for p-channel and 1.2×10^2 kΩ for n-channel) and trap densities. These improvements are mainly attributed to the dual benefits of the high-k Al_2O_3 layer, which enhances electrostatic control through its higher dielectric constant, enabling lower operating voltages, and simultaneously reduces interface trap states at the semiconductor/dielectric interface, facilitating more efficient charge transport. Together, these findings highlight the importance of

dielectric interface engineering for improving both p- and n-type OTFT performance and enabling energy-efficient, low-power organic electronics.

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Author Contributions

WB performed the experiment and wrote manuscript. SW, CLT and HS were involved in analysis, and discussion. DK wrote the manuscript and supervised this work. All authors read and approved the final manuscript.

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Declarations of Competing Interests

The authors declare that they have no competing interests.

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